

TERNA ENGINEERING COLLEGE, NERUL

Title: Academic Schedule (FH-2012)

BRANCH: ELECTRONICS ENGINEERING

CLASS:M.E.-II (ELECTRONICS)

TIME (Hrs)	9:15 10:15	10:15 11:15	11:15 12:15	12:15 13:15	13:15	13:45 14:45	14:45 15:45	15:45 16:45	4:45 5:45
DAY									
THURSDAY	ACT DSB 231	VLSI MZS 231	PE BGH 231	PE BGH 231	RE	VLSI MZS 231	E1-ACT-/SBG		
							E2/VLSI -MZS		
FRIDAY	MS /SVK 231	VLSI MZS 231	ACT DSB 231	ACT DSB 231	CE	PE BGH 231	PICD RDP 231	E1-VLSI-MZS	
								E2-ACT-/SBG	
SATURDAY	MS /SVK 231	MS /SVK 231	E1-MS-/SVK		S	PICD RDP 231	PICD RDP 231	E1-PICD-RPD	
			E2-PICD- BGH					E2-PE-SE	
SUNDAY	E1-PE-BGH				S				
	E2-MS-/SVK								

With effective from: 09/01/2012

MZS Mr. M.Z SHAIKH
 BGH Mr. B.G. HOGADE
 /SVK Mrs. S. KULKARNI
 RDP Mr. R.D. PATANE
 DSB Mr. D.S.BHOSALE
 SE Mr. SAMSUL. EKRAM
 /SBG Mrs S.B. GAIKWAD

VLSI VLSI Design
 PE Process Instrumentation and control design
 MS Microprocessor & Systems-II
 PIDC Process Instrumentation and Circuit design
 ACT Advance Communication Theory
 PE Process Instrumentation and control design
 ACT Advance Communication Theory

Convener
(TIME TABLE)

HOD
(ELECTRONICS ENGG.)

PRINCIPAL