

Design and Simulation of Ternary Logic Based Arithmetic Circuits

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INTRODUCTION

In a VLSI circuit, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to devices [1]. The binary logic is limited due to interconnect which occupies large area on a VLSI chip. In this work, the designs of ternary-valued logic circuits have been explored over multi-valued logic due to the following reasoning. In a numerical system, the number N is given by $N = R^d$ where R is the radix and d is the necessary number of digits up to the next highest integer value where necessary. If the cost or complexity C in any system is assumed to be proportional to $R \times D$ [4], then

$$C = k(R \times d) = k[R (\ln N / \ln R)] \quad (2)$$

where k is some constant. Differentiating with respect to R will show that for a minimum cost C, R should be equal to $e(2.718)$. Since in practice R must be an integer, this suggests that $R=3$ (ternary) would be more economical than $R=2$ (binary) [2]. The present CMOS technology does not use depletion mode transistors. The prime objective in our work is to minimize the number of transistors used, eliminate the use of resistors to lower the power consumption, reduce the propagation delay time and eliminate depletion mode transistors. The reduction in the number of transistors is main focus as that enabled a more compact design which utilized the less chip area. The designs of positive ternary inverter (PTI), negative ternary inverter (NTI) and simple ternary inverter (STI) is based on use of a CMOS inverter and pass

transistors/CMOS transmission gate at its output. The pass transistors at the output of inverter have been used to pull the output node to the required voltage levels and also provide

sufficient equivalent resistance for the ternary logic implementation. The two unary operators PTI and NTI have been used to design a J_k arithmetic circuit, and ternary gate (T-gate) which is essentially a multiplexer. Basically, high-speed and low-power operation of digital circuits could be achieved by reducing both the power supply voltage, V_{DD} and threshold voltage, V_T of MOSFETs [3, 4].

I. TERNARY LOGIC GATES

A. Basic Gates

The most fundamental building blocks in the design of digital systems are the inverter, NOR gate, and NAND gate. In this section, ternary implementations are proposed for the inverter, NOR gate and NAND gate, in which the static power dissipation is low. Three types of basic ternary operations are defined by [5]

$$X_c = \begin{cases} C & \text{if } X = 1 \\ \sqrt{2-X} & \text{if } X = 1 \end{cases} \quad (1)$$

C in Eq. (1) takes the values of logic 1 for a PTI, logic 0 for a STI and logic -1 for a NTI which correspond to higher level (5), middle level (0) and lower level (-5) respectively.

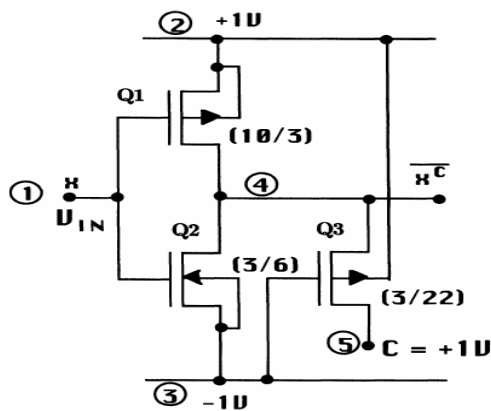


Fig. 1 Positive ternary Inverter

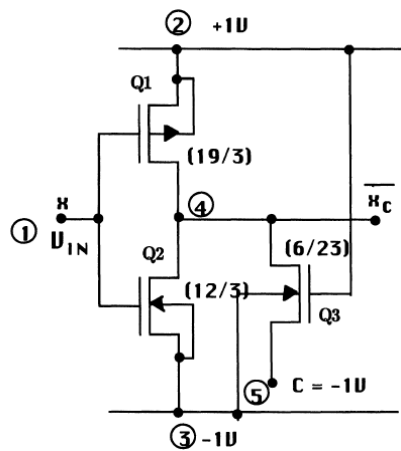


Fig. 2 Negative ternary Inverter

with its gate tied to the positive power supply to keep it constantly turned on. A control signal, C of -IV is applied to the source of n-MOSFET (Q3) and that pulls the output of CMOS inverter to that value. The CMOS inverter is forced to a value of -IV in phase where both transistors of the CMOS inverter are in the cut-off region.

Fig. 3 shows the schematic of a simple ternary inverter (STI) designed by connecting a CMOS transmission gate to the common drain output of a CMOS inverter. The gates of p- and n- MOSFETs (Q3 and Q4) in the transmission gate are tied to negative and positive power supplies, respectively. The transmission gate aids in pulling up a control signal, C of 0V to the output when the inverter is in cut-off.

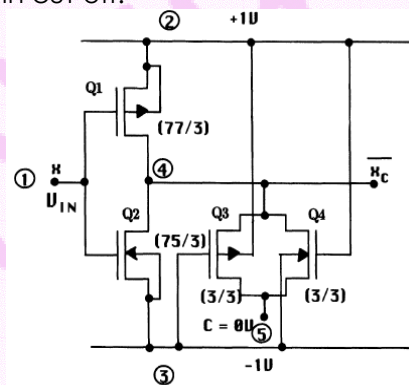


Fig. 3 Simple Ternary Inverter

Fig. 1 shows the schematic of a positive ternary inverter (PTI). A p-MOSFET (Q3) is connected to the output of a standard CMOS inverter. In Fig. 1 the gate of p-MOSFET (Q3) has been tied to the negative power supply to keep it constantly turned on. A control signal, C of + IV is applied to the source of p-MOSFET (Q3). The W/L ratio of p- and n-MOSFETs (Q1 and Q2) in CMOS inverter are 10/3 and 3/6, respectively, and that of p-MOSFET (Q3) connected to the output is 3/22. The p-MOSFET (Q3) pulls the output of the CMOS inverter to + 1V during the cycle where both transistors of the inverter are nearly in cut-off. Fig. 2 shows the schematic of a negative ternary inverter (NTI). An n-MOSFET (Q3) is connected to the output of a CMOS inverter

B. NAND and TNOR

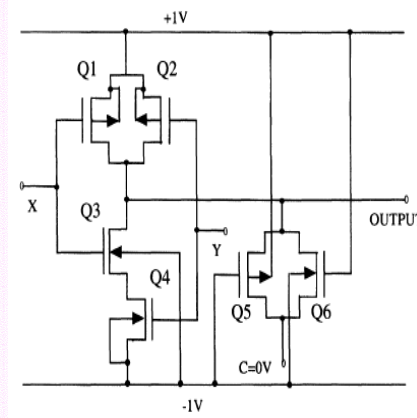


Fig. 4 Ternary NAND (TNAND)

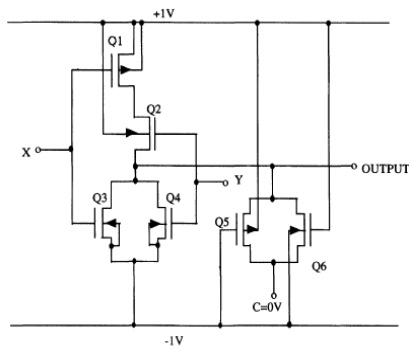


Fig. 5 Ternary NOR (TNOR)

Figures 4 and 5 show the circuits for ternary NAND and ternary NOR, respectively. They are designed by connecting a CMOS transmission gate to the common drain output of a binary CMOS NAND and NOR. The substrate bias connection in MOSFETs of the CMOS inverter is used to apply forward or reverse bias voltage, for the control of threshold voltage and to adjust the transition region in dc voltage transfer characteristics.

II. TERNARY ARITHMETIC CIRCUITS

Based on the ternary operator circuitry described above, it is possible to design simpler and cheaper three-valued logic systems. Examples given are for the J_k arithmetic circuit (decoder) and the three-valued T-gate.

The J_k arithmetic function is defined by

$$Y_k(X) = \begin{cases} 1 & \text{if } X = 1 \\ -1 & \text{if } X = k \end{cases} \quad (2)$$

where k can take values of logic 1, logic 0 and logic -1 which corresponds to higher level (5), middle level (0) and lower level (-5), respectively. The block diagram of a J_k arithmetic circuit (decoder) is shown in Fig. 6 which uses the logic design described [6]. The design of the T-gate circuit is based on the J_k arithmetic circuit. The function of the T-gate is described as follows [5]

$$T(Y_1, Y_2, Y_3; X) = Y_i \quad (3)$$

where i will take a value of 1 if X takes the value of -1, 2 if X is 0, and 3 if X is 1. The block diagram of a T-gate is shown in Fig. 6. Each ternary switch consists of a p-channel and n-channel enhancement transistor. The source of p-channel MOSFET is connected to the drain of n-channel MOSFET and vice versa. A control signal, C controls the n-channel MOSFET directly, and the p-channel MOSFET is controlled by C. When C is equal to +1V the switch will be on, for C equal to -1V the switch will be off. The J_1, J_0, J_{-1} signals of the J_k arithmetic circuits are connected to C of the ternary switch that has inputs Y_1, Y_2, Y_3 , respectively. The value of input to the J_k arithmetic circuit determines which one of the signals (Y_1, Y_2, Y_3) will be steered to the output thus functioning as a multiplexer (encoder).

A. Half Adder

A ternary half adder is a circuit that will add two trits and generate a sum trit and a corresponding carry trit. There are two inputs and two outputs and, consequently, two decoders and two encoders are required. The composite truth table for the circuit can readily be generated as depicted in Table 1.

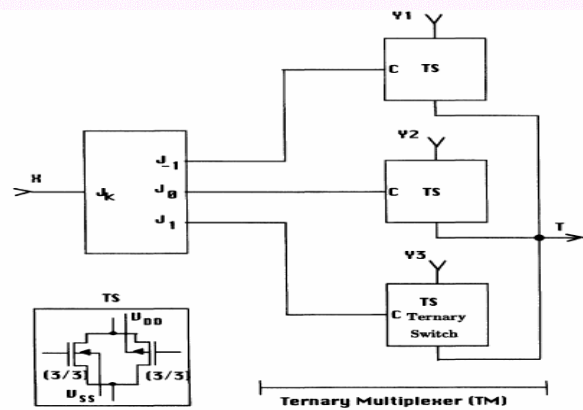


Fig. 6 T-Gate

Table 1 Truth Table for half adder

X	Y	S	C _o
-1	-1	1	-1
-1	0	-1	0
-1	1	0	0
0	-1	-1	0
0	0	0	0
0	1	1	0
1	-1	0	0
1	0	1	0
1	1	-1	1

-1	0	-1	1	-1
-1	0	0	-1	0
-1	0	1	0	0
-1	1	-1	-1	0
-1	1	0	0	0
-1	1	1	1	0
0	-1	-1	1	-1
0	-1	0	-1	0
0	-1	1	0	0
0	0	-1	-1	0
0	0	0	0	0
0	0	1	1	0
0	1	-1	0	0
0	1	0	1	0
0	1	1	-1	1
1	-1	-1	-1	0
1	-1	0	0	0
1	-1	1	1	0
1	0	-1	0	0
1	0	0	1	0
1	0	1	-1	1
1	1	-1	1	0
1	1	0	-1	1
1	1	1	0	1

B. Full Adder

The full adder comprises of fourteen T-gates as shown in Fig. 8. Since the JK arithmetic circuit part of the T-gate is common, we can effectively reduce the component count by making it common for three stages. The area occupied by the ternary adder as a whole can be conserved in this way.

The complete ternary full adder has been simulated using SPICE 9.2 and the corresponding truth table is summarized in Table 2.

Table 2 .Truth Table for Ternary Full Adder

X	Y	C _i	S	C _o
-1	-1	-1	0	-1
-1	-1	0	1	-1
-1	-1	1	-1	0

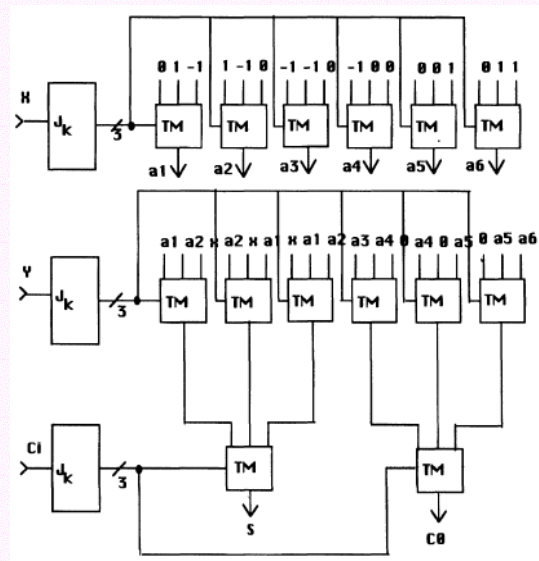


Fig. 7 Ternary Full Adder

III. SIMULATON RESULTS

MICROWIND

MICROWIND is to draw the MOS layout and simulate its behavior. The MICROWIND software works on a lambda grid, not on a micro grid. Consequently same layout may be simulated in any CMOS technology. In this paper CMOS031.rul is used which has 0.2um lambda value. Simulated results from MICROWIND and SPICE are shown below:

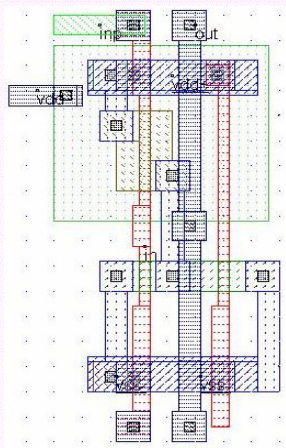


Fig.8 NTI Microwind Layout

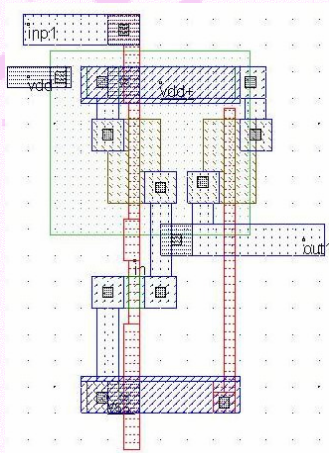


Fig 9 PTI Microwind Layout

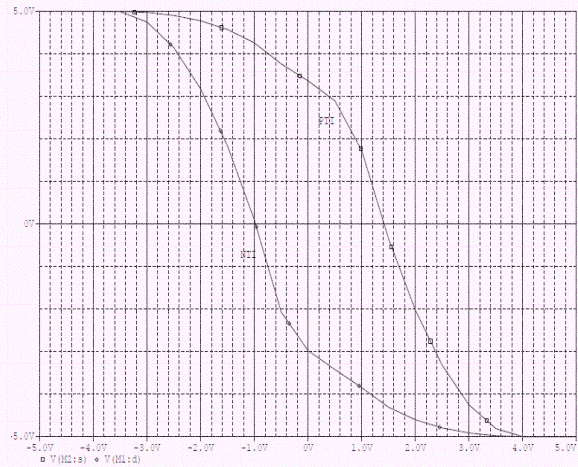


Fig.10 NTI & PTI Characteristic Graph

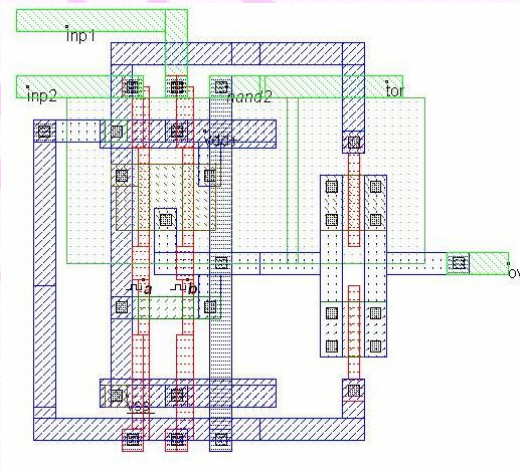


Fig.11 TNAND Microwind Layout

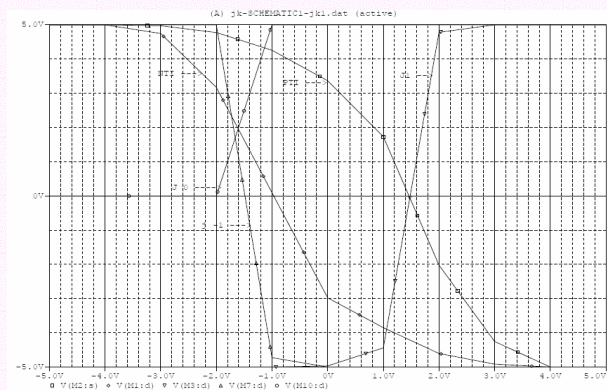


Fig.12 Decoder Characteristic Graph

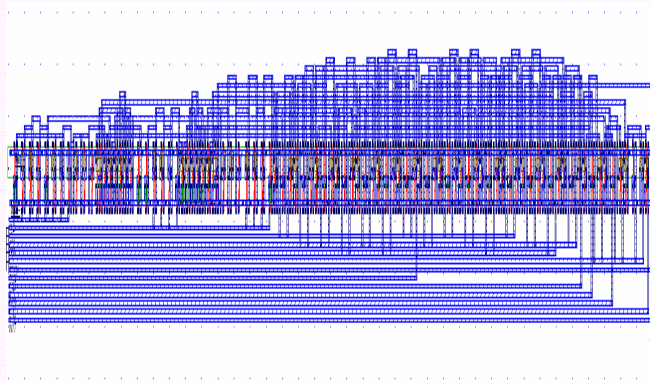


Fig. 13 Microwind Layout for Ternary Half adder

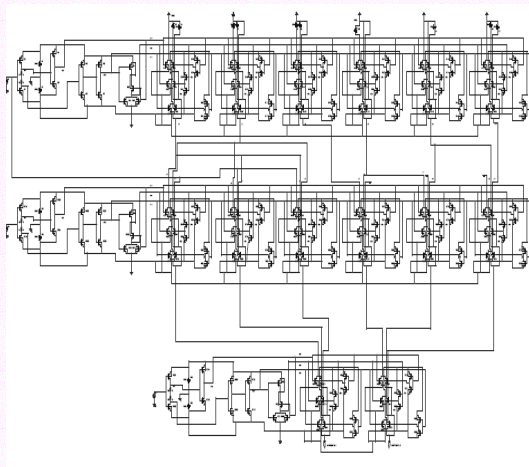


Fig. 14 SPICE Schematic Diagram for Ternary Full adder

Table 3 Power Dissipation

Gate	Present Work	Ref.5
PTI	0.004nW	0.8nW
NTI	$6.67 \times 10^{-5} \text{W}$	12uW
Ternary Full Adder	7.78mW	-
T-Gate	0.2nW	-

IV. CONCLUSION

STI, PTI and NTI have been designed for operation at $\pm 5\text{V}$ power supply voltage. The T-gate uses a J_k arithmetic circuit and three ternary switches. The J_k arithmetic circuit mainly consists of PTI and NTI apart from NOR, inverter and buffer circuits. Half Adder and Full Adder consist of T-gate and J_k arithmetic circuit. The PTI and NTI have been designed using an inverter and pass-transistors at its output. The design of PTI and NTI is fully compatible with current CMOS technology.

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